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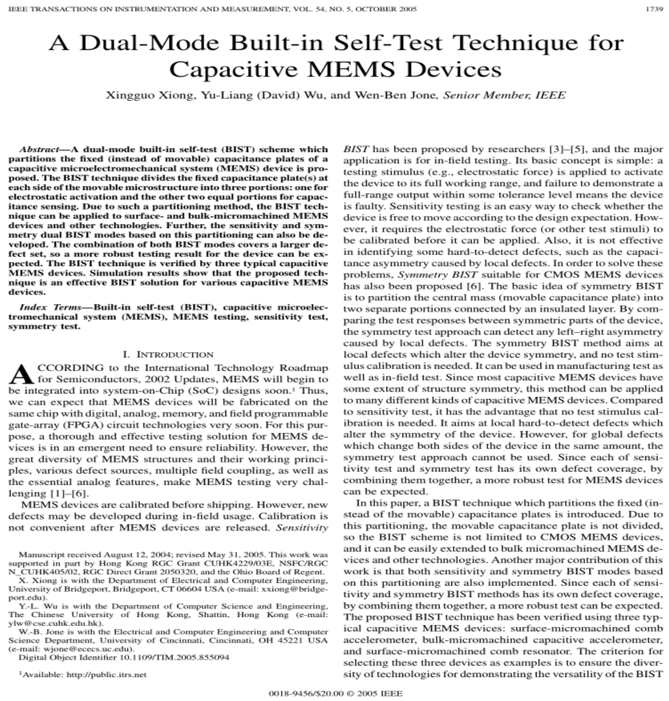

A Dual-Mode Built-in Self-Test Technique for Capacitive MEMS Devices

Xingguo Xiong, Yu-Liang (David) Wu, and Wen-Ben Jone, *Senior Member, IEEE*

***Abstract*—A dual-mode built-in self-test (BIST) scheme which partitions the fixed (instead of movable) capacitance plates of a capacitive microelectromechanical system (MEMS) device is proposed. The BIST technique divides the fixed capacitance plate(s) at each side of the movable microstructure into three portions: one for electrostatic activation and the other two equal portions for capacitance sensing. Due to such a partitioning method, the BIST technique can be applied to surface- and bulk-micromachined MEMS devices and other technologies. Further, the sensitivity and symmetry dual BIST modes based on this partitioning can also be developed. The combination of both BIST modes covers a larger defect set, so a more robust testing result for the device can be expected. The BIST technique is verified by three typical capacitive MEMS devices. Simulation results show that the proposed technique is an effective BIST solution for various capacitive MEMS devices.**

***Index Terms*—Built-in self-test (BIST), capacitive microelectromechanical system (MEMS), MEMS testing, sensitivity test, symmetry test.**

I. INTRODUCTION

ACCORDING to the International Technology Roadmap for Semiconductors, 2002 Updates, MEMS will begin to be integrated into system-on-Chip (SoC) designs soon.[1] Thus, we can expect that MEMS devices will be fabricated on the same chip with digital, analog, memory, and field programmable gate-array (FPGA) circuit technologies very soon. For this purpose, a thorough and effective testing solution for MEMS devices is in an emergent need to ensure reliability. However, the great diversity of MEMS structures and their working principles, various defect sources, multiple field coupling, as well as the essential analog features, make MEMS testing very challenging [1]–[6].

MEMS devices are calibrated before shipping. However, new defects may be developed during in-field usage. Calibration is not convenient after MEMS devices are released. *Sensitivity BIST* has been proposed by researchers [3]–[5], and the major application is for in-field testing. Its basic concept is simple: a testing stimulus (e.g., electrostatic force) is applied to activate the device to its full working range, and failure to demonstrate a full-range output within some tolerance level means the device is faulty. Sensitivity testing is an easy way to check whether the device is free to move according to the design expectation. However, it requires the electrostatic force (or other test stimuli) to be calibrated before it can be applied. Also, it is not effective in identifying some hard-to-detect defects, such as the capacitance asymmetry caused by local defects. In order to solve these problems, *Symmetry BIST* suitable for CMOS MEMS devices has also been proposed [6]. The basic idea of symmetry BIST is to partition the central mass (movable capacitance plate) into two separate portions connected by an insulated layer. By comparing the test responses between symmetric parts of the device, the symmetry test approach can detect any left–right asymmetry caused by local defects. The symmetry BIST method aims at local defects which alter the device symmetry, and no test stimulus calibration is needed. It can be used in manufacturing test as well as in-field test. Since most capacitive MEMS devices have some extent of structure symmetry, this method can be applied to many different kinds of capacitive MEMS devices. Compared to sensitivity test, it has the advantage that no test stimulus calibration is needed. It aims at local hard-to-detect defects which alter the symmetry of the device. However, for global defects which change both sides of the device in the same amount, the symmetry test approach cannot be used. Since each of sensitivity test and symmetry test has its own defect coverage, by combining them together, a more robust test for MEMS devices can be expected.

In this paper, a BIST technique which partitions the fixed (instead of the movable) capacitance plates is introduced. Due to this partitioning, the movable capacitance plate is not divided, so the BIST scheme is not limited to CMOS MEMS devices, and it can be easily extended to bulk micromachined MEMS devices and other technologies. Another major contribution of this work is that both sensitivity and symmetry BIST modes based on this partitioning are also implemented. Since each of sensitivity and symmetry BIST methods has its own defect coverage, by combining them together, a more robust test can be expected. The proposed BIST technique has been verified using three typical capacitive MEMS devices: surface-micromachined comb accelerometer, bulk-micromachined capacitive accelerometer, and surface-micromachined comb resonator. The criterion for selecting these three devices as examples is to ensure the diversity of technologies for demonstrating the versatility of the BIST

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X. Xiong is with the Department of Electrical and Computer Engineering, University of Bridgeport, Bridgeport, CT 06604 USA (e-mail: xxiong@bridgeport.edu).

Y.-L. Wu is with the Department of Computer Science and Engineering, The Chinese University of Hong Kong, Shattin, Hong Kong (e-mail: ylw@cse.cuhk.edu.hk).

W.-B. Jone is with the Electrical and Computer Engineering and Computer Science Department, University of Cincinnati, Cincinnati, OH 45221 USA (e-mail: wjone@ececs.uc.edu).

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